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Azadet 10-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kameran Azadet, Erich Franz Haratsch
Case: 10-2
Serial No.: 09/471,920
Filing Date: December 23, 1999
Title: Method and Apparatus For Shortening the Critical Path of Reduced Complexity Sequence Estimation Techniques
Group: 2739
Examiner: To Be Assigned

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following document listed on the accompanying PTO Form 1449. A copy of the listed item is enclosed.

1. Fettweis et al., "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture," IEEE Communications Magazine, May 1991.
2. Chevillat et al., "Decoding of Trellis-Encoded Signals in the Presence of Intersymbol Interference and Noise," IEEE Transactions on Communications, Vol. 37, No. 7, July 1989.
3. Erich F. Haratsch, "High-Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA.
4. K. Azadet, "Gigabit Ethernet over Unshielded Twisted Pair Cables," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA.
5. Black et al., "A 140-Mb/s, 32-State, Radix-4 Viterbi Decoder," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992.
6. Cypher et al. "Generalized Trace-Back Techniques for Survivor Memory Management in the Viterbi Algorithm*," Journal of VLSI Signal Processing, 5, 85-94(1993).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,

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Date: February 15, 2000

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